We Claim:

1. A test structure for determining an extent of a doping region of outer capacitor electrodes of trench capacitors in a memory cell array, the trench capacitors of the memory cell array being arranged in matrix form and each having a trench with an inner capacitor electrode isolated by a dielectric layer from an outer capacitor electrode, formed as a doping region, around a lower trench region, the test structure comprising:

first and second contact-connectible capacitor plates;

a first row of trench capacitors formed with outer capacitor electrodes electrically connected to said first capacitor plate, and a second row of trench capacitors disposed parallel to said first row of trench capacitors and formed with outer capacitor electrodes electrically connected to said second capacitor plate;

in a plan view, at least one trench capacitor of said first row of trench capacitors and at least one trench capacitor of said second row of trench capacitors each having a lengthened basic area on a side facing the respective other row of said trench capacitors and overlapping the respectively other lengthened basic areas.

2. The test structure according to claim 1, formed in a kerf region on a semiconductor wafer.

3. The test structure according to claim 1, wherein a basic area of at least one further trench capacitor of said second row of trench capacitors is lengthened on the side facing said first row, forming an interleaved comb structure together with said at least one trench capacitor of said first row and said at least one trench capacitor of said second row having the lengthened basic areas, wherein said trench capacitor with the lengthened basic area of said first row of trench capacitors is spaced equidistantly from said two trench capacitors with the lengthened basic areas of said second row of trench capacitors.

4. A test structure pattern, comprising a multiplicity of test structures according to claim 3, with different said test structures having different spacings between said two outer trench capacitors with the lengthened basic areas of said second row of trench capacitors and said central trench capacitor with the lengthened basic area of said first row of trench capacitors.